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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
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Erik K. Norden

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EXAMINER

COLEMAN, ERIC

ART UNIT

PAPER NUMBER

2183

4

DATE MAILED: 05/12/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

# Office Action Summary

Application No.

09/878,145

Applicant(s)

NORDEN ET AL.

Examiner

Eric Coleman

Art Unit

2183

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

## Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

## Status

- 1) ☐ Responsive to communication(s) filed on \_\_\_\_.
- 2a) ☐ This action is **FINAL**. 2b) ☒ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

## Disposition of Claims

- 4) ☒ Claim(s) 1-23 is/are pending in the application.
- 4a) Of the above claim(s) \_\_\_\_ is/are withdrawn from consideration.
- 5) ☐ Claim(s) \_\_\_\_ is/are allowed.
- 6) ☒ Claim(s) 1-23 is/are rejected.
- 7) ☐ Claim(s) \_\_\_\_ is/are objected to.
- 8) ☐ Claim(s) \_\_\_\_ are subject to restriction and/or election requirement.

## Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☐ The drawing(s) filed on \_\_\_\_ is/are: a) ☐ accepted or b) ☐ objected to by the Examiner.  
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).  
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

## Priority under 35 U.S.C. § 119

- 12) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☐ All b) ☐ Some \* c) ☐ None of:
1. ☐ Certified copies of the priority documents have been received.
2. ☐ Certified copies of the priority documents have been received in Application No. \_\_\_\_.
3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

\* See the attached detailed Office action for a list of the certified copies not received.

## Attachment(s)

- 1) ☒ Notice of References Cited (PTO-892)
- 2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
- 3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08)  
Paper No(s)/Mail Date \_\_\_\_.
- 4) ☐ Interview Summary (PTO-413)  
Paper No(s)/Mail Date. \_\_\_\_.
- 5) ☐ Notice of Informal Patent Application (PTO-152)
- 6) ☐ Other: \_\_\_\_.

**DETAILED ACTION**

***Claim Rejections - 35 USC § 112***

1. The following is a quotation of the second paragraph of 35 U.S.C. 112:

The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

2. Claim 17 is rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

3. The scope of meaning of issuing a third instruction from the first pipeline stage to the first pipeline stage (claim 17, lines 1-3) is unclear (i.e., what operation is occurring since the instruction in a pipeline stage is being issued to the same stage).

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(a) the invention was known or used by others in this country, or patented or described in a printed publication in this or a foreign country, before the invention thereof by the applicant for a patent.

4. Claims 1,2,5-8 are rejected under 35 U.S.C. 102(a) as being anticipated by Dowling (patent No. 6,157,988).

5. Dowling taught the invention as claimed including a data processing ("DP") system comprising:

- a) First pipeline stage (210) (e.g., fig. 7);

b) First expansion stage (712) coupled to the first pipeline stage (210) (e.g., see fig.7); and

c) Second pipeline stage (212) coupled to the first pipeline stage (210) and the first expansion stage (712), wherein the second pipeline stage is configured to selectively receive instructions from the first pipeline stage or the first expansion stage (e.g., see fig. 7 and col. 15, lines 1-64).

6. As per claim 2, Dowling taught a multiplexer (718) coupled between the first expansion stage (712) and the second pipeline stage (212) and between the first pipeline stage (210) and the second pipeline stage (212) (e.g., see fig. 7).

7. As per claim 5, Dowling taught a third pipeline stage (214) coupled to the second pipeline stage (212)(e.g., see fig. 7).

8. As per claim 6,7 the Dowling first pipeline stage was part of an instruction fetch and decode unit that comprised a instruction fetch stage (202,204,206,208) coupled to the first pipeline stage (210) (e.g., see fig. 7).

9. As per claim 8, the Dowling second pipeline stage comprised a decode stage (212) (e.g., see fig. 7).

### ***Claim Rejections - 35 USC § 103***

10. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the

invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

11. Claims 9 is rejected under 35 U.S.C. 103(a) as being unpatentable over Dowling (patent No. 6,157,988).

12. Dowling taught the invention substantially as claimed including a data processing ("DP") system comprising:

a) First pipeline state (210) (e.g., fig. 7);

b) First expansion stage (712) coupled to the first pipeline stage (210) (e.g., see fig.7); and

c) Second pipeline stage (212) coupled to the first pipeline stage (210) and the first expansion stage (712), wherein the second pipeline stage is configured to selectively receive instructions from the first pipeline stage or the first expansion stage (e.g., see fig. 7 and col. 15, lines 1-64).

13. As per claim 2, Dowling taught a multiplexer (718) coupled between the first expansion stage (712) and the second pipeline stage (212) and between the first pipeline stage (210) and the second pipeline stage (212) (e.g., see fig. 7).

14. As per claim 5, Dowling taught a third pipeline stage (214) coupled to the second pipeline stage (212)(e.g., see fig. 7).

15. As per claim 6,7 the Dowling first pipeline stage was part of an instruction fetch and decode unit that comprised a instruction fetch stage (202,204,206,208) coupled to the first pipeline stage (210) (e.g., see fig. 7).

16. As per claim 8, the Dowling second pipeline stage comprised a decode stage (212) (e.g., see fig. 7).

17. Dowling did not specifically detail (claim 9) that the pipeline was configured to process integer instructions. However Dowling taught the use of RISC or Digital signal processing pipelines (e.g., see col. 9, lines 56-60). Therefore since prior art processors that performed RISC processing were capable to performing integer operations one of ordinary skill in the DP art would have been motivated to configure the system to process integer instructions at least in order to provide compatibility with existing programs.

18. Claims 3,4, are rejected under 35 U.S.C. 103(a) as being unpatentable over Dowling as applied to claims 1-2 above, and further in view of Olson (patent No. 5,878,242).

19. As per claim 3, Olson taught a second expansion stage (102) coupled the first pipeline stage (104) and the first expansion stage (130) via and wherein the first expansion stage is configured to selectively receive instructions from the first pipeline stage (104) or the second expansion stage (102).

20. It would have been obvious to one of ordinary skill in the DP art at the time of claimed invention to combine the teachings of Dowling and Olson. One of ordinary skill would have been motivated to incorporate the Olson teaching of plurality of additional pipeline stages that were selectively connected to the pipeline in order to allow more flexibility in placing instructions in any location in the pipeline to reduce delays in processing (e.g., see col. 2, lines 35-50 of Olson).

21. Further as per claim 4, Olson taught a multiplexer (122,124,126) coupled between the second expansion stage (102) and the first expansion stage (130) and

between the first pipeline stage (104) and the first expansion stage (130) (e.g., see fig. 3).

***Claim Rejections - 35 USC § 102***

22. Claims 1,10,11-16,18-23 are rejected under 35 U.S.C. 102(a) as being anticipated by Munson (patent No. 6,408,377).

23. Munson taught the invention as claimed including a data processing ("DP") system comprising:

- a) First pipeline stage (203);
- b) First expansion stage (217) coupled to the first pipeline stage (203); and
- c) Second pipeline stage (87) coupled to the first pipeline stage (203) and the first expansion stage (217), wherein the second pipeline stage is configured to selectively receive instructions from the first pipeline stage or the first expansion stage (e.g., see fig. 2A,2B,6A,6B and col. 9, line 61-col. 10, line 64).

24. Munson also taught (claim 10) issuing a first instruction from the first pipeline stage to the second pipeline stage (e.g., see fig. 2A,2B,6A,6B and col. 9, line 61-col. 10, line 64). if the second pipeline stage can accept the first instruction and (claims 10,11,12,18) issuing a first instruction to the first expansion stage when the second pipeline stage cannot accept the first instruction or is full and issuing a second instruction to the second expansion stage and a (claim 16) issuing a next instruction to the first expansion stage when the first instruction leaves the first expansion stage (e.g., see col. 9, line 61-col. 10, line 64).

25. As per claims 13-15,20 Munson taught sending the instructions from the first pipeline stage and/or second expansion stage and then from one expansion stage to the next expansion stage in a pipelined manner when the corresponding expansion stage could receive it (e.g., see col. 9, line 61-col. 10, line 39 and fig. 4).

26. As per claim 19 Munson taught a multiplexer (243) (e.g., see fig. 6a) coupled between the first pipeline stage (203)(e.g., see fig. 4) and the second pipeline stage (87) and between the first pipeline stage (203) and the second pipeline stage (e.g., see figs. 4,6).

27. As per claims 21,22,23, Munson taught a multiplexer (229) coupled between the second expansion stage (218) and a first expansion stage (217) and between the first pipeline stage (203) and second pipeline stage (87) (e.g., see fig. 4) and third pipeline stage coupled to the second pipeline stage (e.g., figs. 6a, 6b) wherein the pipeline is part of an instruction fetch and issue unit (e.g., see figs. 2a, 4).

### ***Conclusion***

28. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

Johnson (patent No. 5,976,972) disclosed a system for performing microcode paging during instruction execution in an instruction processor (e.g., see abstract).

Fernando (patent No. 6,272,616) disclosed a system for executing multiple instruction streams in a digital processor with multiple data paths (e.g., see abstract).

Molnar (patent No. 5,937,177) disclosed a system control for an asynchronous pipeline (e.g., see abstract and figs. 1,2,3,4).




Any inquiry concerning this communication or earlier communications from the examiner should be directed to Eric Coleman whose telephone number is (703) 305-9674. The examiner can normally be reached on Monday-Thursday.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Eddie Chan can be reached on (703) 305-9712. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

EC

  
ERIC COLEMAN  
PRIMARY EXAMINER

April 30, 2004